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Method of Making Hybrid Semiconductor – Magnetic Spin Based Memory

RELATED APPLICATION DATA

The present invention claims priority to and is a continuation of application serial no. 10/100,210 filed March 18, 2002 entitled "Magnetoelectronic Memory Element With Inductively Coupled Write Wires," (now U.S. Patent 6,741,494). Application serial No. 10/100,210 is a continuation of an application serial no. 09/532,076 filed March 22, 2000 titled "Magnetoelectronic Memory Element With Isolation Element" (now U.S. Patent 6,388,916). The latter application serial no. 09/532,076 is in turn a divisional application of serial no. 08/806,028 filed February 24, 1997 entitled "Hybrid Hall Effect Memory Device & Method of Operation," now U.S. Patent No. 6,064,083. Serial no. 08/806,028 is a continuation-in-part of serial no. 08/643,805, filed May 6, 1996 titled "Hybrid Hall Effect Device and Method of Operation," (now U.S. Patent No. 5,652,445), which in turn is a continuation-in-part of an application serial no. 08/493,815, filed June 21, 1995 titled "Magnetic Spin Transistor Hybrid Circuit Element," (now U.S. Patent No. 5,565,695); and said serial no. 08/806,028 is also a continuation-in-part of an application serial no. 08/425,884, filed April 21, 1995 titled "Magnetic Spin Transistor, Logic Gate & Method of Operation," (now U.S. Patent No. 5,629,549); ~~and an application serial no. 08/643,804 filed May 6, 1996 titled "Magnetic Spin Injected Field Effect Transistor and Method of Operation," (now U.S. Patent No. 5,654,566),~~ and an application serial no. 08/643,804 filed May 6, 1996 titled "Magnetic Spin Injected Field Effect Transistor and Method of Operation," (now U.S. Patent No. 5,654,566).

The above applications and materials are expressly incorporated by reference herein.